Introduction to Intel oneAPI for HPC and AI-DL

OneAPI – 가속 컴퓨팅을 개발하기 위한 스마트한 방식

intel software

2020. 1. 21. MOASYS

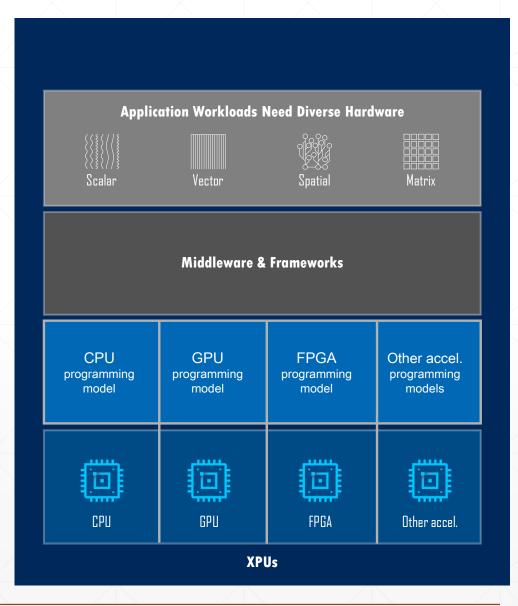


Outline

- What is oneAPI?
- Intel oneAPI DPC++ Programming
- High-performance computing (HPC)
- Machine learning, Deep learning, and analytics

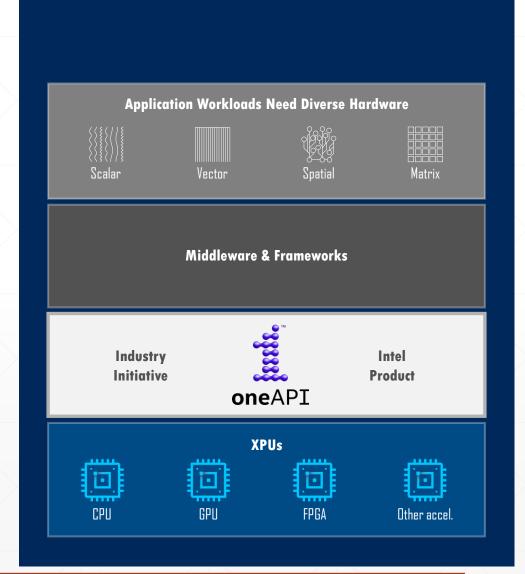
Programming Challenges for Multiple Architectures

- Growth in specialized workloads
- Variety of data-centric hardware required
- Separate programming models and toolchains for each architecture are required today
- Software development complexity limits freedom of architectural choice



oneAPI: One Programming Model for Multiple Architectures and Vendors

- Freedom to Make Your Best Choice
 - Choose the best accelerated technology the software doesn't decide for you
- Realize all the Hardware Value
 - Performance across CPU, GPUs, FPGAs, and other accelerators
- Develop & Deploy Software with Peace of Mind
 - Open industry standards provide a safe, clear path to the future
 - Compatible with existing languages and programming models including C++, Python, SYCL, OpenMP, Fortran, and MPI

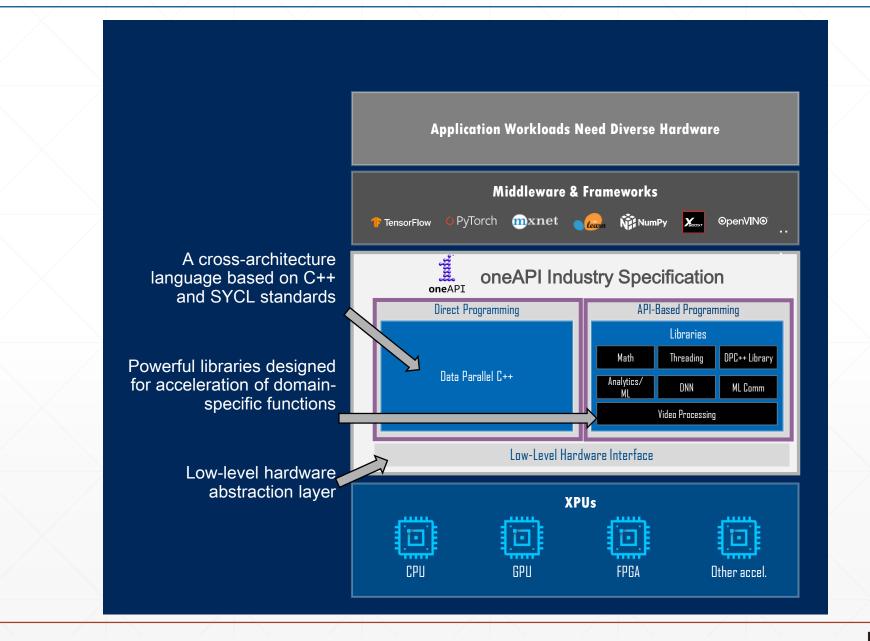


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oneAPI Industry Initiative: Break the Chains of Proprietary Lock-in

 Open to promote community and industry collaboration

 Enables code reuse across architectures and vendors



Data Parallel C++: Standards-based, Cross-architecture Language

- Freedom of Choice: Future-Ready Programming Model
 - Allows code reuse across hardware targets
 - Permits custom tuning for a specific accelerator
 - Open, cross-industry alternative to proprietary language
- DPC++ = ISO C++ and Khronos SYCL and community extensions
 - Delivers C++ productivity benefits, using common, familiar C and C++ constructs
 - Adds SYCL from the Khronos Group for data parallelism and heterogeneous programming
- Community Project Drives Language Enhancements
 - Provides extensions to simplify data parallel programming
 - Continues evolution through open and cooperative development

DPC++ = **ISO C++** and Khronos SYCL and community extensions

	P rogramm Parallel (-	
Commur	nity Exten	sions	
Khrc	onos SYCI	_	
IS	50 C++		

DEVICE SELECTOR

- The device_selector class enables the runtime selection of a particular device to execute kernels based upon user-provided heuristics.
- The following code sample shows use of the standard device selectors(default_selector, cpu_selector, gpu_selector...) and a derived device_selector

```
default_selector selector;
```

```
// host_selector selector;
```

```
// cpu_selector selector;
```

```
// gpu_selector selector;
```

```
queue q(selector);
```

```
std::cout << "Device: " << q.get_device().get_info<info::device::name>() << std::endl;</pre>
```

- QUEUE
 - A queue submits command groups to be executed by the SYCL runtime
 - Queue is a mechanism where work is submitted to a device.
 - A Queue map to one device and multiple queues can be mapped to the same device.

```
queue q;
q.submit([&](handler& h) {
    // COMMAND GROUP CODE
});
```



KERNEL

- The kernel class encapsulates methods and data for executing code on the device when a command group is instantiated
- Kernel object is not explicitly constructed by the user
- Kernel object is constructed when a kernel dispatch function, such as parallel_for, is called

```
q.submit([&](handler& h) {
```

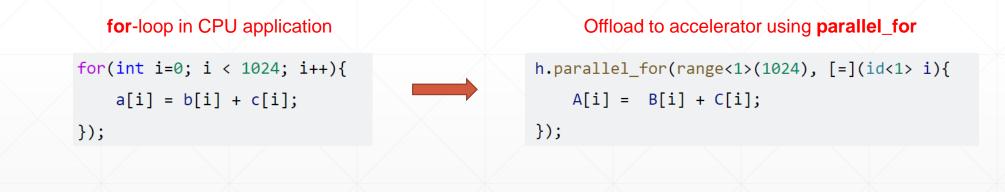
```
h.parallel_for(range<1>(N), [=](id<1> i) {
```

```
A[i] = B[i] + C[i]);
```

```
});
```

```
});
```

- Parallel Kernels
 - Parallel Kernel allows multiple instances of an operation to execute in parallel.
 - Useful to offload parallel execution of a basic for-loop in which each iteration is completely independent and in any order.
 - Parallel kernels are expressed using the parallel_for function

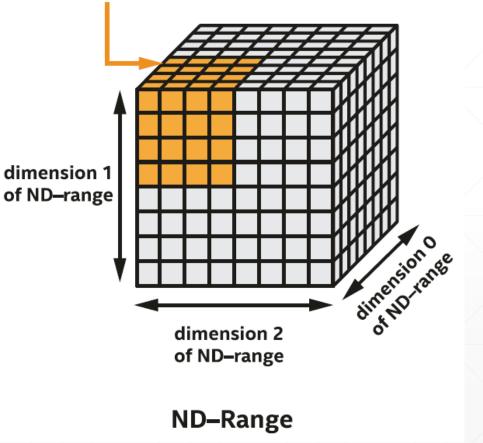


- Basic Parallel Kernels
 - The functionality of basic parallel kernels is exposed via range, id and item classes
 - range class used to describe the iteration space of parallel execution
 - id class is used to index an individual instance of a kernel in a parallel execution
 - item class represents an individual instance of a kernel function, exposes additional functions to query properties of the execution range

```
h.parallel_for(range<1>(1024), [=](id<1> idx){
    // CODE THAT RUNS ON DEVICE
});
h.parallel_for(range<1>(1024), [=](item<1> item){
    auto idx = item.get_id();
    auto R = item.get_range();
    // CODE THAT RUNS ON DEVICE
});
```

- ND-Range Kernels
 - Basic Parallel Kernels are easy way to parallelize a for-loop but does not allow performance optimization at hardware level.
 - ND-Range kernel is another way to expresses parallelism which enable low level performance tuning by providing access to local memory and mapping executions to compute units on hardware.





- Intel DPC++ Compatibility Tool
 - Minimizes Code-Migration Time
 - Assists developers migrating code written in CUDA to DPC++ by generating DPC++ code wherever possible
 - Expect up to 80-90% of code to migrate automatically
 - Inline comments are provided to help developer complete code

Intel[®] DPC++ Compatibility Tool Usage Flow

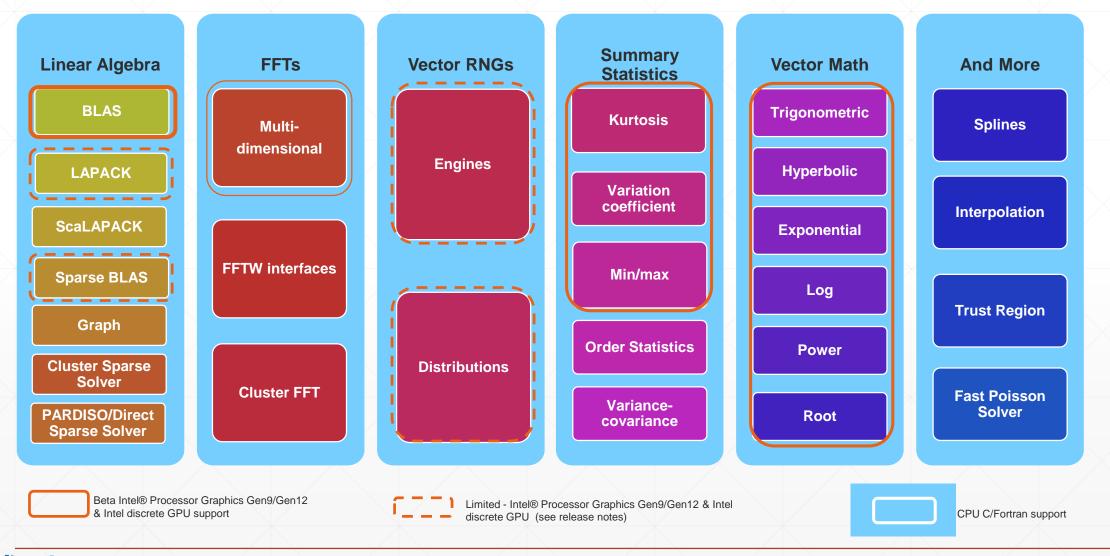


\$ dpct vector_add.cu
\$ dpcpp vector_add.dp.cpp



<pre>#include <cuda.h> #include <stdio.h> #define VECTOR_SIZE 256</stdio.h></cuda.h></pre>	<pre>#include <cl sycl.hpp=""> #include <dpct dpct.hpp=""> #include <stdio.h> #define VECTOR_SIZE 256</stdio.h></dpct></cl></pre>	Header
global void VectorAddKernel(float* A, float* B, float* C) Idx 0 1 2 259 { A[threadIdx.x] = threadIdx.x + 1.0f; B[threadIdx.x] = threadIdx.x + 1.0f; C[threadIdx.x] = A[threadIdx.x] + B[threadIdx.x]; } C 2 4 6 512	<pre>A[item_ct1.get_local_id(2)] = item_ct1.get_local_id(2) + 1.0f; B[item_ct1.get_local_id(2)] = item_ct1.get_local_id(2) + 1.0f; C[item_ct1.get_local_id(2)] = A[item_ct1.get_local_id(2)] + B[item_ct1.get_local_id(2)];</pre>	Kernel definition CUDA: 1D SYCL: 3D (general)
<pre>int main() { float *d_A, *d_B, *d_C; </pre>	<pre>int main() { dpct::device_ext &dev_ct1 = dpct::get_current_device(); sycl::queue &q_ct1 = dev_ct1.default_queue(); float *d_A, *d_B, *d_C;</pre>	Device selection Queue intialization
<pre>cudaMalloc(&d_A, VECTOR_SIZE*sizeof(float)); cudaMalloc(&d_B, VECTOR_SIZE*sizeof(float)); cudaMalloc(&d_C, VECTOR_SIZE*sizeof(float));</pre>	<pre>d_A = sycl::malloc_device<float>(VECTOR_SIZE, q_ct1); d_B = sycl::malloc_device<float>(VECTOR_SIZE, q_ct1); d_C = sycl::malloc_device<float>(VECTOR_SIZE, q_ct1);</float></float></float></pre>	USM allocation
<pre>VectorAddKernel<<<1, VECTOR_SIZE>>>(d_A, d_B, d_C);</pre>	<pre>q_ct1.submit([&](sycl::handler &cgh) { cgh.parallel_for(sycl::nd_range<3>(sycl::range<3>(1, 1, VECTOR_SIZE), // global</pre>	Kernel execution CUDA: 1 thread block SYCL: 1 work group
<pre>float Result[VECTOR_SIZE] = { }; cudaMemcpy(Result, d_C, VECTOR_SIZE*sizeof(float), cudaMemcpyDeviceToHost); cudaFree(d_A); cudaFree(d_B); cudaFree(d_C);</pre>	<pre>float Result[VECTOR_SIZE] = { }; q_ct1.memcpy(Result, d_C, VECTOR_SIZE * sizeof(float)).wait(); syc1::free(d_A, q_ct1); syc1::free(d_B, q_ct1); syc1::free(d_C, q_ct1);</pre>	Data movement Deallocation
<pre>for (int i = 0; i < VECTOR_SIZE; i++) { if (i % 16 == 0) { printf("\n"); } printf("%f ", Result[i]); }</pre>	<pre>for (int i = 0; i < VECTOR_SIZE; i++) { if (i % 16 == 0) { printf("\n"); } printf("%f ", Result[i]); }</pre>	Generic C code No migration
return 0; } ntel software	return 0; }	moasys

Intel oneMKL



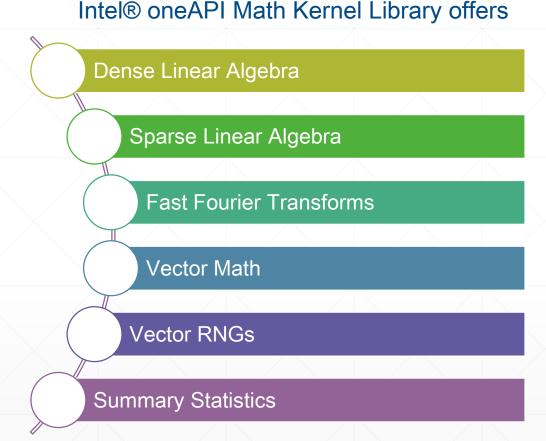
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Intel oneMKL

Accelerate Math Processing, Increase Application Performance

- Language support for DPC++ and Intel® C & Fortran compilers
- Available at no cost and royalty-free
- Great performance with minimal effort
- Full support for CPUs and select support for Intel® Processor Graphics Gen9, Gen12, and discrete Intel® GPUs
- Speeds computations for scientific, engineering, and financial applications by providing highly optimized, threaded, and vectorized math functions
- Provides key functionality for dense and sparse linear algebra (BLAS, LAPACK, PARDISO), FFTs, vector math, summary statistics, splines, and more
- Dispatches optimized code for each processor automatically without the need to branch code
- Optimized for single-core vectorization and cache utilization
- Automatic parallelism for multi-core CPUs, GPUs, and scales from core to clusters

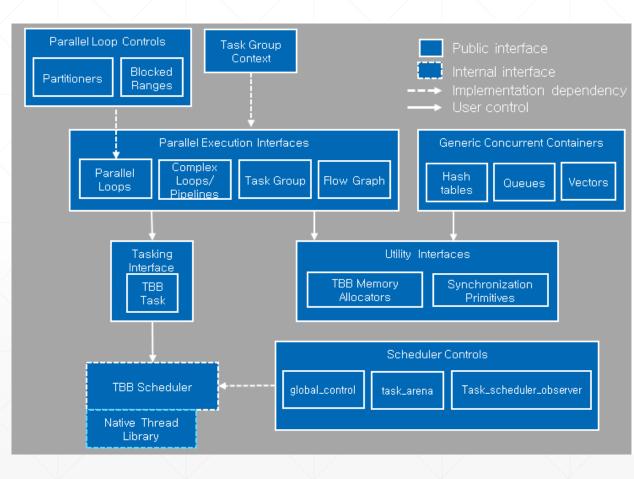


Intel oneTBB

Advanced Scaling for Fast Applications

- Flexible C++ Library for Parallelism
 - An easy way for developers to express parallelism in applications without the need to have deep hardware knowledge
- Future Proof & Scale Application Performance
 - Effectively parallelize and scale performance for computationally intensive workloads on current and future platforms
- Compatible with Other Threading Packages
 - Keep legacy code as-is and use oneTBB for new implementations. Seamlessly coexist with other threading packages
- Simplified and Enhanced Application Composability
 - Create composable, scalable parallelism on the CPU, and extendable with enhanced handling of accelerators

- oneTBB Architecture Overview
 - A Collection of Building Blocks to Develop Highly Scalable Threaded Applications
 - Includes high-level parallel execution interfaces
 - Parallel Loops: parallel_for, parallel_reduce, etc.
 - Complex Algorithms: pipelines, task groups
 - Flow Graph: Expressing data flow independent graphs
 - All build on top of TBB tasks, these tasks execute on top of the TBB scheduler
 - Scheduler controls & parallel loops controls to tightly control performance
 - Concurrent Containers Queues, Vectors, etc. are thread safe and thread friendly
 - Scalable memory allocator, synchronization primitives



Intel® MPI Library: Flexible, Efficient and Scalable Cluster Messaging

Optimized MPI Application Performance

- Application-specific tuning
- Automatic tuning
- Support for latest Intel® Xeon® Scalable Processors

Lower Latency and Multi-vendor Interoperability

- Industry-leading latency
- Performance-optimized support for the fabric capabilities through OpenFabrics Interfaces (OFI)

Faster MPI Communication

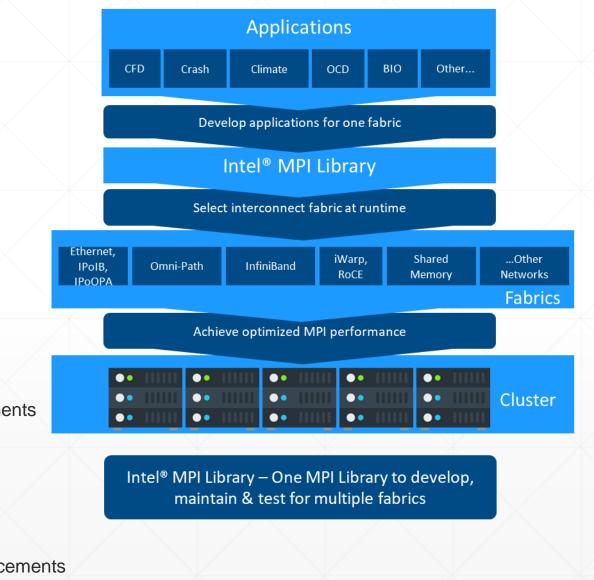
Optimized collectives

Sustainable scalability

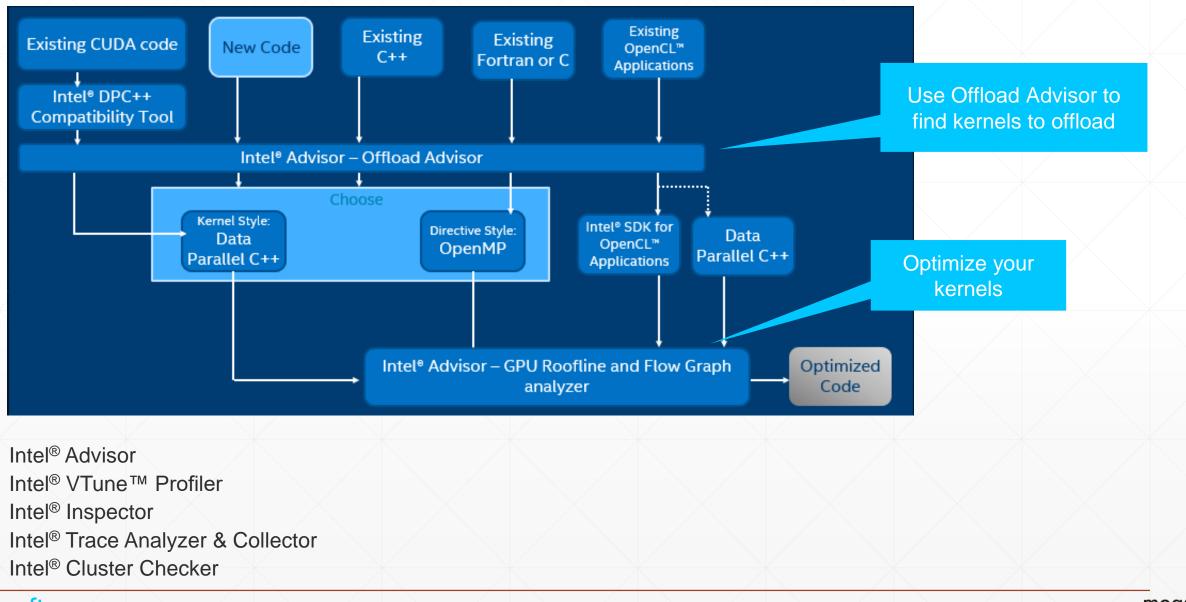
- Native InfiniBand interface support allows
- Lower latencies, higher bandwidth, reduced memory requirements

Key Updates

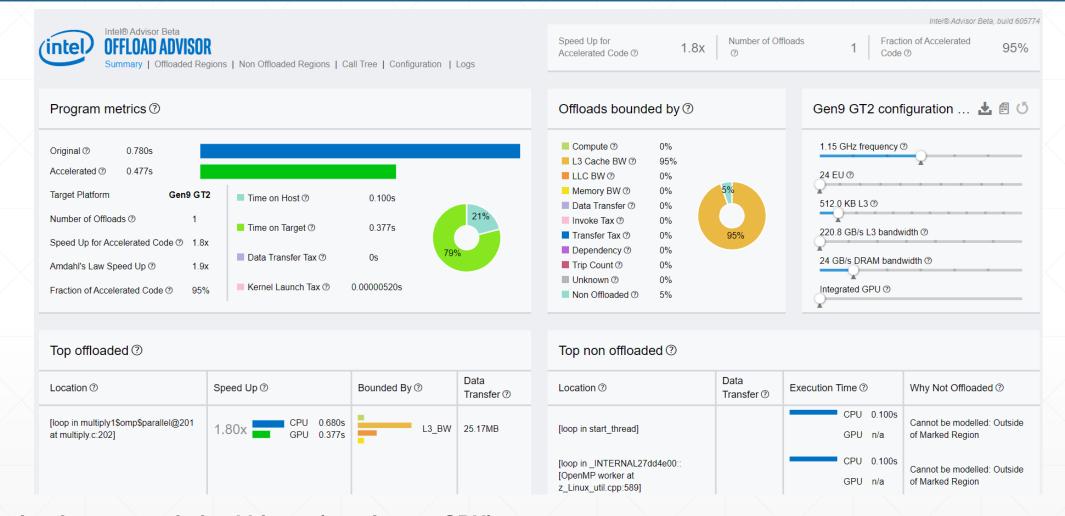
- Intel® GPU pinning support
- Distributed Asynchronous Object Storage (DAOS) support
- Intel® Xeon® Platinum processor 92XX optimizations
- Mellanox ConnectX: 3/4/5/6 (FDR/EDR/HDR) support enhancements



Using Intel Analysis Tools to Increase Performance



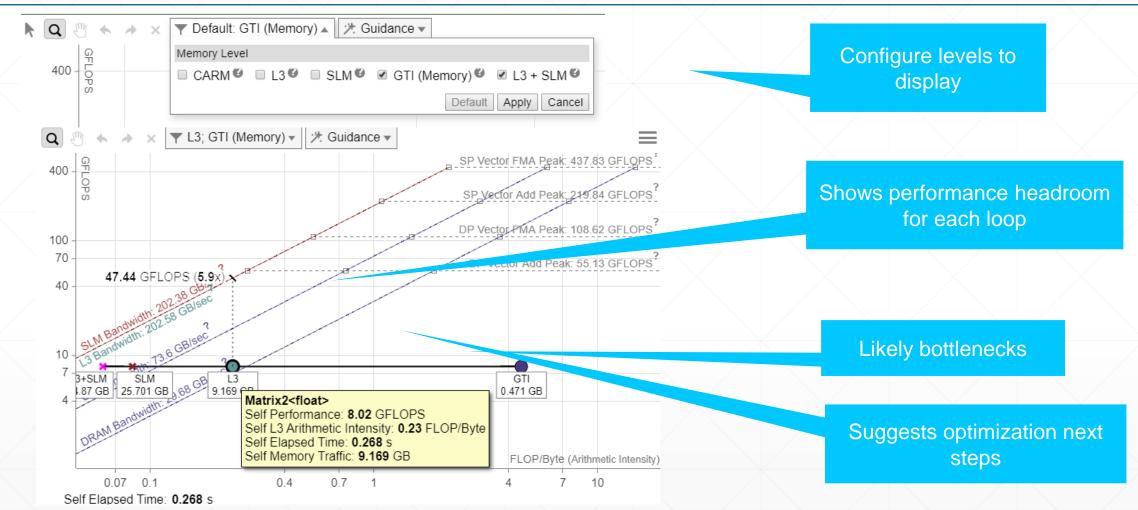
Intel® Advisor - Offload Advisor: Efficiently offload code to GPUs



Starting from an optimized binary (running on CPU)

- Identify high-impact opportunities to offload
- Detect bottlenecks and key bounding factors
- Get your code ready even before you have the hardware by modeling performance, headroom, and bottlenecks

Intel[®] Advisor - GPU Roofline: Find effective optimization strategies



Quickly find & fix performance bottlenecks, realize all the value of your hardware

- See performance headroom against hardware limitations
- Determine performance optimization strategy by identifying bottlenecks and which optimizations will pay off the most
- Visualize optimization progress

Intel[®] VTune[™] Profiler: Analyze and Tune Application Performance

Save Time Optimizing Code

- Accurately profile C, C++, Fortran, Python, Go, Java
- Optimize CPU, threading, memory, cache, storage
- Take advantage of <u>Priority Support</u>[†]

What's New in 2021.1 Release (partial list)

- Production release of Platform Profiler
- Design & optimize for Intel® Optane[™] DC Persistent Memory
- Application Performance Snapshot
 - Add communication-pattern diagnosis
 - Profile more ranks
- Linux
 - Extensive perf-enables analysis without adding drivers

Analysis Configuration	Collection Log	Summary	Bottom-up	Caller/Callee	Top-dowr	n Tree	Platform	
Grouping: Function / Call S	Stack							• 🛠 D
			CP	U Time 🔻			«	[]
Function / Call Stack			>	Spin	Time	~	>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>	Microarchitecture
FUNCTION / Call Stack		Time by Utilizat Ok 🚦 Ideal		Imbalance or Serial Spinning	Lock Contention	Other	Overhead Time	Usage
grid_intersect	3.490s			0s	0s	0s	0s	37.79
sphere_intersect	3.004s			0s	0s	0s	0s	41.69
GdipDrawImagePointRe	0.431s 📕			0s	0s	0s	0s	100.09
grid_bounds_intersect	0.176s 📒			0s	0s	0s	0s	27.99
func@0x6b101e50	0.130s 📕			0s	0s	0s	0s	10.99
<pre>kmp_fork_barrier</pre>	0s			0.057s	0s	0.064s	0.001s	100.09
▶ < _kmp_launch_threa	Os			0.055s	0s	0.064s	0.001s	100.09
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OMP Worker Thread #1	1 (TI							cktick Sample
OMP Master Thread #0) (TI 🚺 🎽						CPU Tir	ne
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Intel[®] VTune[™] Profiler: GPU Architecture Summary

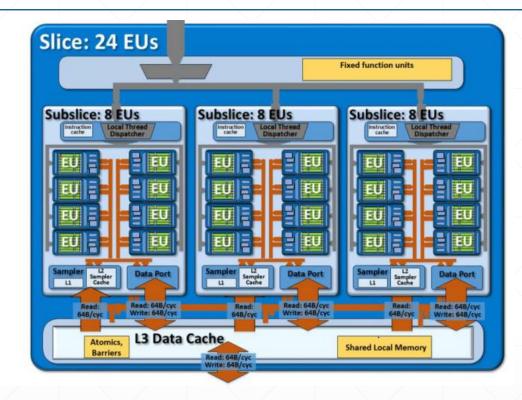
Collection and Platform Info

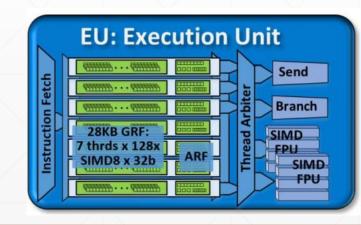
~	0011
(\vee)	GPU
\sim	

Name:	Intel(R) UHD Graphics 620
Vendor:	Intel Corporation
Driver:	27.20.100.8187
EU Count:	24
Max EU Thread Count:	7
Max Core Frequency:	1.1 GHz
Version:	OpenCL C 2.0
Max Compute Units	24
Max Work Group Si	ze: 256
Local Memory:	64 KB
SVM Capabilities:	Fine-grained buffer with atomics

Intel Gen9 GPU details:

- 24EU x 7thr = 168 threads
- 128 General-Purpose Registry File (GRF) of 32 bytes
- 2 SIMD-4 FPU of 32-bit FP or INT data
- 16 MAD/cycle (ADD+MUL) x 2FPUs x SIMD-4
- 2 additional units: Branch and Send





Intel[®] VTune[™] Profiler: Optimize Your GPU Usage

GPU Offload (Preview) GPU Offload (Preview) Image: The transmission of tr	GPU Compute/Media Hotspots (preview) Analysis Configuration Collection Log Summary Architecture Dagram Pautom GPU GPU Stallect: 32.5% k Idle: 0.0% Stallect: 32.5% k Stallect: 32.5% k Stallect	Graphics 0.0% 0.00 GB/s 2 0.00 GB/s Write	L3 8e+8 Misses/ Miss Ratio 33 SLM	s	GTI		System DRAM			INTEL VTU	JNE PROF	LER	
 Packet Queue Depth Histogram Packet Duration Histogram 	CPU Utilization: 0.0%												
⊘ Hottest GPU Computing Tasks	Grouping: Computing Task										• 🔨	0 %	
This section lists the most active computing tasks running on the GPU, sorted by the Total Time. Focus on the computing tasks flagged as performance-critical.	Computing Task	Work Size Global V Local	Total Time	Average Time	Computing Tas		SVM Usage Type		Transferred		Array	dle	
The sector has an most date comparing date termining of the St of control of an total time. Focus of an comparing date hugges to performance endedi.	MatrixMultiply2	4096 x 4096	5,440s	5.440s	1 1	31WD Widd1	SVM Osage Type	3120	Iotal, Obrsec		32.5%	0.0%	
Computing Task Total Time Total Compute Time Total Transfer Time (f)	▶ clEnqueueReadBufferRect		0.012s	0.012s	1							4.4%	
Matrix <fioat> ► 3.980s 0.961s 3.019s</fioat>	[Outside any task]									20.9% 1	10.4%	58.8%	

Quickly Find & Fix Performance Bottlenecks

0.000s

0.000s

- Explore code execution on your platform's various CPU and GPU cores
- Identify whether your application is GPU- or CPU-bound

0.000s

GPU offload:

clEngueueReadBufferRect

*N/A is applied to non-summable metrics

- Identifying how effectively your application uses DPC++ or OpenCL kernels
- Exploring GPU usage and analyzing a software queue for GPU engines at each moment of time

GPU hotspots:

- Analyze the most time-consuming GPU kernels, characterize GPU usage based on GPU hardware metrics
- GPU code performance at the source-line level and kernel-assembly level

Intel[®] Inspector: Locate & Debug Threading, Memory Errors

Find and eliminate

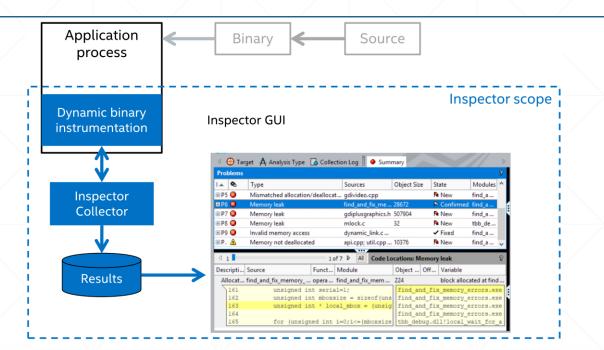
- Memory leaks, invalid access
- Persistent memory errors
- Races & deadlocks
- C, C++ and Fortran (or a mix)

Simple, Reliable, Accurate

- No special recompiles: use any build, any compiler
- Analyzes dynamically generated or linked code
- Inspects 3rd party libraries without source
- Command line for automated regression analysis

Faster Diagnosis with Debugger Breakpoints

- Breakpoint set just before the problem occurs
- Examine variables and threads with the debugger



Features	Memory Analysis	Threading Analysis	Persistence Memory	
View context of problem Stack Multiple Contributing Source Locations	\checkmark	√ √	√ √	
Collapse multiple "sightings" to one error	\checkmark	\checkmark	\checkmark	
Suppress, Filter, Workflow Management	\checkmark	\checkmark	\checkmark	
Visual Studio Integration (Windows)	\checkmark	\checkmark	\checkmark	
Command line for automated tests	\checkmark	\checkmark	\checkmark	
Timeline visualization	\checkmark	\checkmark		
Memory growth during a transaction	\checkmark			
Trigger debugger breakpoints	\checkmark	\checkmark		

Intel® Trace Analyzer & Collector: Profile & Analyze MPI Application

Mechanism	Advantages	Disadvantages
Run with -trace	un with <i>-trace</i> Automatic collection of MPI calls No medication to source, compile or lihnk	
Link with -trace	Automatic collection of MPI calls	No collection of user code Must be done at link time
Compile with -tcollect	Automatic collection of all functions entries/exits	Requires code re-compilation
Add API calls	Selective collection of desired code sections	Requires code modification

Debug MPI applications:

- GDB
- Allinea DDT
- gtool

Scale MPI applications:

- Scale performance: perform on more nodes
- Scale forward: multi-core ready
- Scale efficiently: tune and debug on more nodes

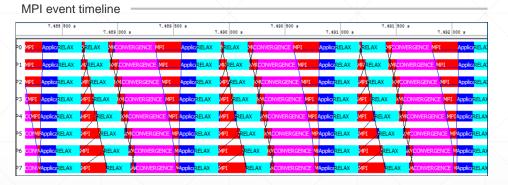
Analyze, tune & optimize:

- Identify communication hotspots
- Evaluate profiling statistics and load balancing
- Visualize and understand parallel application behavior
- Analyze common MPI issues

Top MPI functions This section lists the most active MPI functions from all MPI calls in the application. MPI_Sendrecv 0.0643 sec (8.59 %) MPI_Allreduce 0.0415 sec (5.54 %) MPI Finalize 0.00785 sec (1.05 %)

MPI_Bcast MPI_Errhandler_create





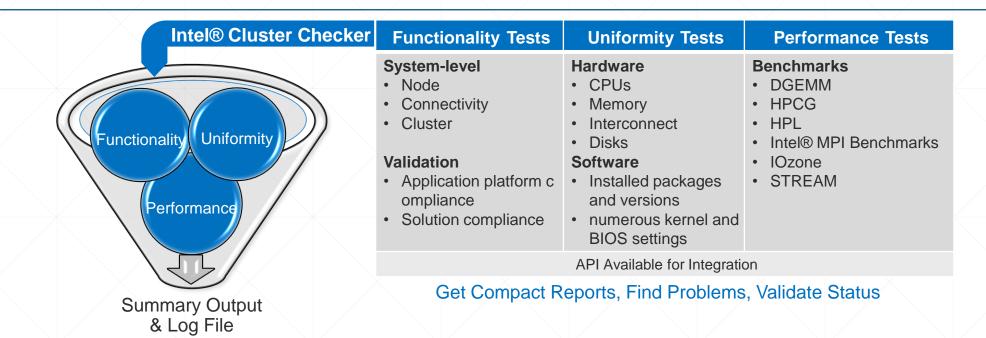
MPI correctness checking

PO		PLBarier NPLBarier	1
P1	And Recy Subdisbuilding Enne	MP_Banier MMP_Banier MMMP_Finalze	
P2	APP_Int 00 000000 00 PC Inte	PLBaie MPLBaie NYMPLFindize	
P3	AND Recy NR BAR BAR BAR BAR BAR BAR BAR BAR BAR BA	Req.MPI_Ba Recv MPI_Barrier MMMPI_Finalize	
P4		HPLBarier MMPLBarier NMMPLFinalize	
P5	NUR PREV MR PREMI	Request, IMF Recv MPLBN MMPL Finalize	
P6	Alf-Lised Lised Lised Lised Lised Lise Lised Lised Lised Lised		
P7	NAMP, Recy MP, Recy	Request, free Recv NYMPL_Finalize	
1		*	1

warnings

errors

Intel[®] Cluster Checker: Functionality, Uniformity & Performance Tests



Comprehensive pre-packed cluster systems expertise out-of-the-box

- Suitable for HPC experts and those new to HPC
- Tests can be executed in selected groups on any subset of nodes

Certifying, Testing, and Troubleshooting Clusters

- Check over 100 characteristics that may affect operation and performance
- Catch issues, identify details or remedies
- Use for better uptime and productivity
- Free download, can be redistributed

Priority Support available for Intel® oneAPI Base & HPC Toolkits in commercial versions

Intel oneAPI AI Analytics Toolkit

Speed Up Development with open AI software



		lachin	ie le	earnin	ANALYTICS ZOO	Dee Model Zoo	p learning OpenVINO
Developers librarie S Data Scientists	Intel [®] Data Analytics Acceleration Library (DAAL)	Intel [®] Distribution for Python* (Sklearn*, Pandas*)	R (Cart, RandomF orest, e1071)	Distributed (MILib on Spark, Mahout)	Big[mxne	et O PyTon work optimizations in	
Kernel Library Developers	S Int	el [®] Math Kerne (Intel [®] MKL)			Comm	oneAPI Collectiv unication Librar Intel® oneCCL)	1.11
isit: www.intel.ai	/technology			CPU -	GPU		

1 An open source version is available at: 01.org/openvinotoolkit *Other names and brands may be claimed as the property of others. Developer personas show above represent the primary user base for each row, but are not mutually-exclusive All products, computer systems, dates, and figures are preliminary based on current expectations, and are subject to change without notice.

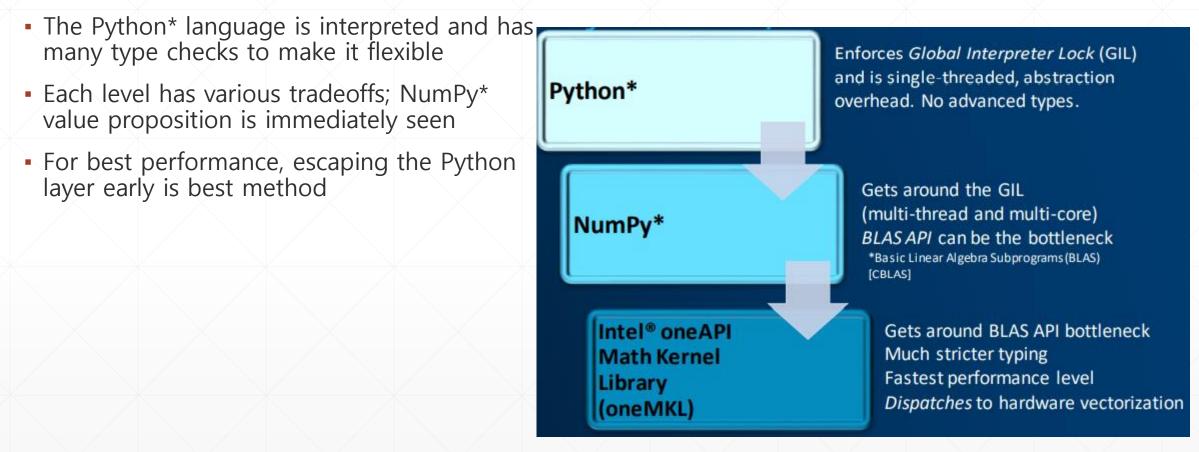
Accelerate libraries with Intel® Distribution for Python*

- High Performance Python for Scientific Computing, Data Analytics, Machine Learning

Faster Performance	Greater Productivity	Ecosystem compatibility
Performance Libraries, Parallelism, Multithreading, Language Extensions	Prebuilt & Accelerated Packages	Supports Python* 2.7 & 3.6, & 3.7 conda, pip
Accelerated NumPy*/SciPy*/scikit-learn* with oneMKL ¹ & oneDAL ² Data analytics, machine learning with scikit-	Prebuilt & optimized packages for numerical computing, machine/deep learning, HPC & data analytics	Compatible & powered by Anaconda*, supports conda & pip Distribution & individual optimized packages also
learn, daal4py Optimized run-times Intel MPI®, Intel® TBB	Drop-in replacement for existing Python* Usually NO code changes required!	oneMKL accelerated NumPy*, and SciPy now in Anaconda*!
Scale with Numba* & Cython* Includes optimized mpi4py, works with Dask*& PySpark*	Conda build recipes included in packages Free download & free for all uses including	Optimizations upstreamed to main Python* trunk Commercial support through Intel® Parallel
Optimized for latest Intel® architecture Intel® Architecture Platforms	commercial deployment	Studio XE
Operating System: Windows*, Linux*, MacOS ¹	*	

Performance Optimization

The layers of quantitative Python*



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Installing Intel® Distribution for Python* 2020

\geq	Standalone Installer	Download full installer from https://software.intel.com/en-us/intel-distribution-for-python	
	Anaconda.org Anaconda.org/intel channel	<pre>> conda configadd channels intel > conda install intelpython3_full > conda install intelpython3_core</pre>	
	РуРІ	<pre>pip install intel-numpy intel-scipy intel-sckit-learn https://software.intel.com/en-us/articles/installing-the-intel-distribution-for-python-and-intel- performance-libraries-with-pip-and</pre>	2.7 & 3.6 & 3.7
7	Docker Hub	docker pull intelpython/intelpython3_full	
>	YUM/APT	Access for yum/apt: https://software.intel.com/en-us/articles/installing-intel-free-libs-and-python	

OneAPI Deep Neural Network Library (OneDNN)

• Features:

 API: DPC++, C++, and C Training: float32, bfloat16 Inference: float32, float16, bfloat16, int8 MLPs, CNNs (1D, 2D and 3D), RNNs (plain, LSTM, GRU) 	Category	Functions
	Compute intensive operations	 (De-)Convolution Inner Product Vanilla RNN, LSTM, GRU
 Support matrix: Compilers: Intel, GCC, CLANG, MSVC OSes: Linux*, Windows* CPU engine: HW: Intel Atom®, Intel® Core™, Intel® Xeon® Runtimes: DPC++, OpenMP, TBB GPU engine: 	Memory bandwidth limited operations	 Pooling Batch Normalization Local Response Normalization Elementwise (ReLU, tanh, logistic etc.) Softmax Sum Concat Shuffle
 HW: Intel[®] HD Graphics, Intel[®] Iris[®] Plus Graphics Runtimes: DPC++, OpenCL[™] 	Data manipulation	• Reorder

OneAPI Deep Neural Network Library (OneDNN)

What's Inside



Deep learning and AI ecosystem includes edge and datacenter applications.

- Open source frameworks (TensorFlow^{*}, Pytorch^{*}, ONNX Runtime^{*})
- OEM applications (Matlab^{*}, DL4J^{*})
 - Cloud service providers internal workloads
 - Intel deep learning products (OpenVINO[™], BigDL)

oneDNN is an open source performance library for deep learning applications

- Includes optimized versions of key deep learning functions
- <u>Abstracts out</u> instruction set and other complexities of performance optimizations
- Same API for both Intel CPU's and GPU's, use the best technology for the job
- <u>Open</u> for community contributions

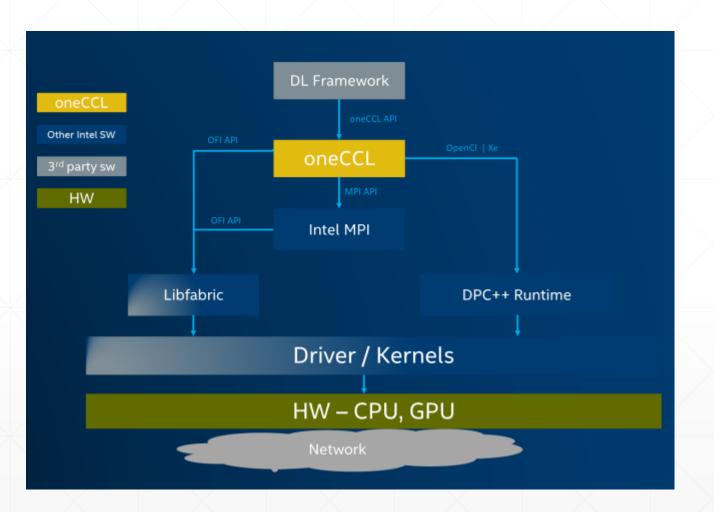
Optimization Notice: Intel's compilers may or may not optimize to the same degree for non-Intel microprocessors for optimizations that are not unique to Intel microprocessors. These optimizations include SSE2, SSE3, and SSSE3 instruction sets and other optimizations. Intel does not guarantee the availability, functionality, or effectiveness of any optimization on microprocessors not manufactured by Intel. Microprocessor-dependent optimizations in this product are intended for use with Intel microprocessors. Certain optimizations not specific to Intel microarchitecture are reserved for Intel microprocessors. Please refer to the applicable product User and Reference Guides for more information regarding the specific instruction sets covered by this notice. Notice Revision #20110804

Intel oneAPI Collective Communications Library (OneCCL)

- Optimized communication patterns cross nodes
 - Provides optimized communication patterns for high performance on Intel® CPUs and GPUs to distribute model training across multiple nodes
- support many interconnects
 - such as Intel® Omni-Path Architecture, InfiniBand*, and Ethernet
- On top of MPI and libfabrics
 - Built on top of lower-level communication middleware MPI and libfabrics
- All –gather, all-reduce for Deep Learning
 - Enables efficient implementations of collectives used for deep learning training all-gather, allreduce

Intel oneAPI Collective Communications Library (OneCCL)

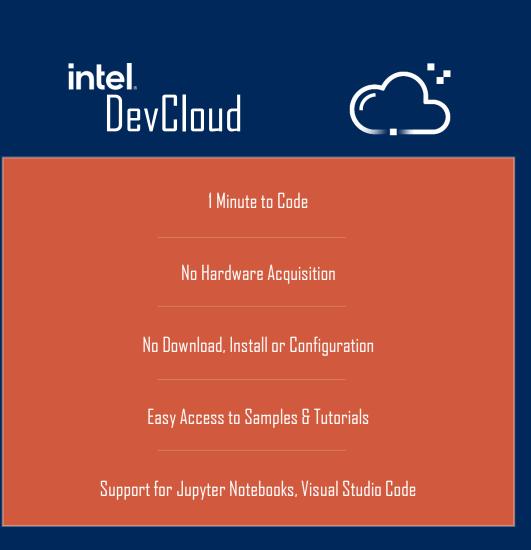
- Provides optimized communication patterns for high performance on Intel® CPUs and GPUs to distribute model training across multiple nodes
- Transparently supports many interconnects, such as Intel® Omni-Path Architecture, InfiniBand*, and Ethernet
- Built on top of lower-level communication middleware – MPI and libfabrics



Introduction to Intel Devcloud

oneAPI available now on Intel[®] DEVCLOUD

- A development sandbox to develop, test and run your workloads across a range of Intel CPUs, GPUs, and FPGAs using Intel's oneAPI software
- software.intel.com/devcloud/oneapi
- A Fast Way to Start Coding
 - Try the oneAPI toolkits, compilers, performance libraries, and tools
 - Get 120 days of free access to the latest Intel[®] hardware and oneAPI software



Summary

- Diverse workloads are driving the need for heterogeneous compute architectures, but each architecture has required separate programming models.
- oneAPI cross-architecture programming model provides freedom of choice. Apply your skills to the next innovation, not to rewriting software for the next hardware platform.
- Intel® oneAPI products take full advantage of accelerated compute by maximizing performance across Intel CPUs, GPUs, and FPGAs.
- Develop confidently with a proven set of cross-architecture libraries and advanced tools that interoperate with existing performance programming models.

THANK YOU